Electrical transport properties of individual gallium nitride nanowires synthesized by chemical-vapor-deposition

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We have synthesized high-quality gallium nitride (GaN) nanowires by a chemical-vapor-deposition method and studied the electrical transport properties. The electrical measurements on individual GaN nanowires show a pronounced *n*-type field effect due to nitrogen vacancies in the whole measured temperature ranges. The *n*-type gate response and the temperature dependence of the current–voltage characteristics could be understood by the band bending at the interface of the metal electrode and GaN wire. The estimated electron mobility from the gate modulation characteristics is about 2.15 $cm^2/V\,s$ at room temperature, suggesting the diffusive nature of electron transport in the nanowires. © *2002 American Institute of Physics.*
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Various molecular-scale devices based on the carbon nanotube (CNT) have been realized recently, such as field-effect transistors,[1] single electron transistors,[2] heterojunctions,[3] and crossed junctions.[4] However, there might be some critical limitations difficult to overcome in CNT-based electronic devices. First, precisely selective growth of metallic or semiconducting tubes, i.e., controlling chiralities of the nanotube is still difficult. Second, controlled and long-term stable doping of CNTs is also a very challenging topic. Instead of the CNT, synthesized various kinds of nanowires, for example, Si, GaN, and GaAs, seem to be able to overcome the fundamental limitations of the CNT as mentioned above.[5,6] Nanowires are mostly inherently semiconducting and relatively easy to dope with suitable impurities through conventional semiconductor technology.

The GaN nanowire is one of the most promising elemental building blocks in nanotechnological applications. GaN nanowires with a large band gap and structural confinement have great potential for use as nanosized UV or blue emitters, detectors, high-speed field-effect transistors, and high-temperature microelectronic devices.[7–9] Recently, there have been several reports on the synthesis of GaN nanowires by arc-discharge, laser-assist catalytic growth, direct reaction of the mixture, etc.[10–16] Huang *et al.* also reported successful fabrication of logic gates and demonstrated the computation capabilities from assembled nanowire *p*-Si and *n*-GaN crossed nanowire junctions.[6] Here, we report the synthesis of the high-crystalline structure of GaN nanowires by the thermal chemical-vapor-deposition (CVD) method and studied the temperature-dependent electrical transport properties of GaN nanowires with Au/Ti metal electrodes.

High-quality GaN wires were synthesized using a Ni catalyst by direct reaction of the mixture of gallium metal and GaN powder with flowing ammonia at 1000 °C using thermal CVD. This method is very simple and can homogeneously produce a large quantity of GaN nanowires with high purity on a large area. A typical scanning electron microscope (SEM) image of the synthesized GaN nanowires is shown in Fig. 1(a). It shows that high-purity GaN nanowires are uniformly distributed with high yields on the alumina substrate. The GaN nanowires have lengths up to several hundred micrometers and diameters in the range of 30–70 nm. The inset shows the magnified SEM image of the GaN nanowires, revealing straight nanowires with high purity and no catalyst particle at the tip. Figure 1(b) is a transmission electron microscope (TEM) image of a single GaN nanowire showing the single-crystalline structure. The inset in the upper-right-hand corner of Fig. 1(b) is an electron diffraction pattern of the nanowire, which can be indexed to the diffraction of wurtzite GaN[0001]. The result shown in Fig. 1(b) indicates that the GaN nanowire is a single-crystal hexagonal wurtzite structure. We analyzed x-ray diffraction pattern for GaN nanowires to investigate the overall crystal structure and phase purity of the nanowires. The diffraction peaks clearly appeared at 2 theta values of 32.37, 34.52, and 36.86, respectively. It reveals that synthesized nanowires have high purity of the GaN wurtzite phase.

An individual GaN nanowire was prepared on a Si substrate with a 500-nm-thick thermally grown SiO_2 layer. The patterns for the electrical leads were generated, using electron-beam lithography, onto the selected GaN nanowire and then 20 nm of Ti and 50 nm of Au were deposited successively on the contact area by thermal evaporation. The upper inset of Fig. 2 shows the SEM image of a GaN wire with five Ti/Au electrodes attached to it. The diameter of the nanowire is about 30 nm. To form stable electrical contacts between the GaN nanowire and Ti/Au electrodes, we have performed rapid thermal annealing at 400–500 °C for 30 s.

Figure 2 shows the temperature dependence of the current–voltage ($I-V$) characteristics between electrodes 2

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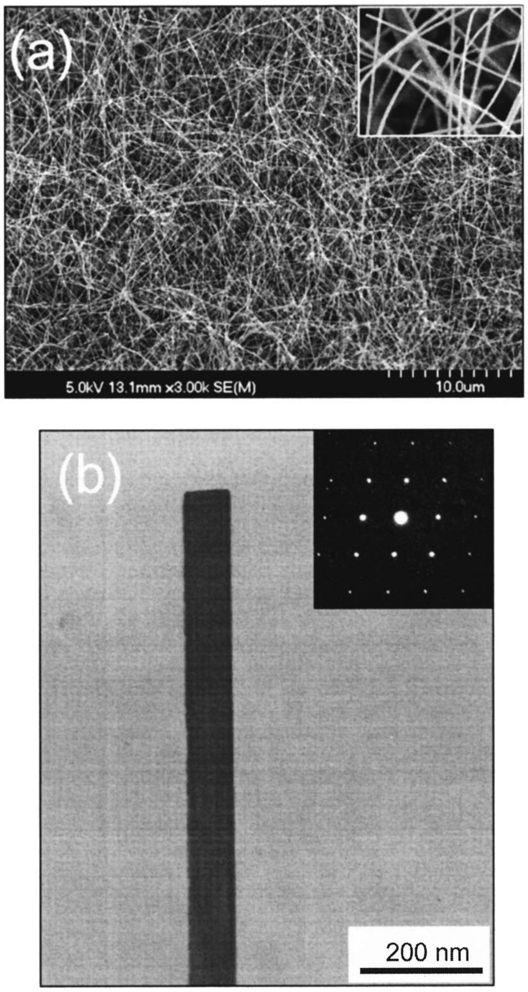

FIG. 1. (a) Typical SEM image of the synthesized GaN nanowires. Inset: magnified SEM image of GaN nanowires. (b) TEM image of a single GaN nanowire showing a single-crystalline structure. Inset: electron diffraction pattern of the nanowire, which can be indexed to the diffraction of wurtzite GaN[0001].

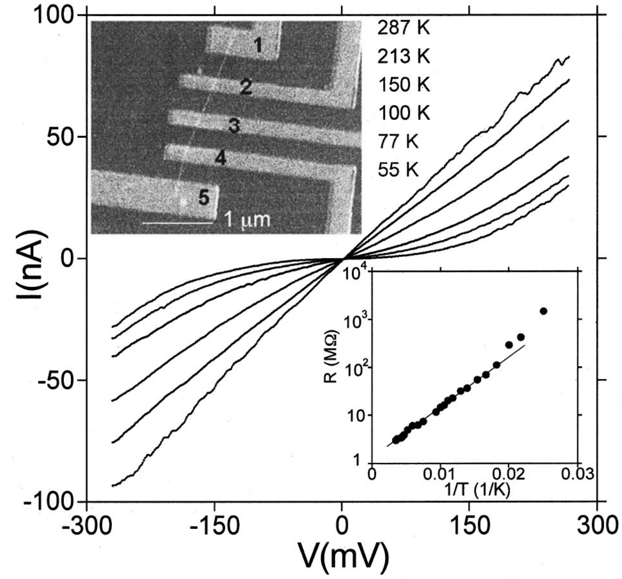

FIG. 2. Temperature-dependent $I-V$ curves of a GaN nanowire between electrodes 2 and 3. The measured temperatures were 283, 213, 150, 100, 77, and 55 K from above the curve. Inset: SEM image of the sample in this study. Numbers in the image represent Ti/Au electrodes for electrical measurement (upper figure). Resistance as a function of inverse temperature ($1/T$) between the electrodes 2 and 3 (lower figure).

and 3 at zero gate voltage. Measurements with other electrodes also show similar behavior but with different resistances. The linear resistance increases from 3 to 14 MΩ as the temperature is lowered from 280 to 100 K. The temperature-dependent resistance at zero bias voltage can be fitted to the thermal activation form, $\exp(-E_a/k_BT)$ with the activation energy of $E_a=20.9$ meV at the high-temperature region, as shown in the lower inset of Fig. 2.

For further clarification of the electrical transport properties of the nanowire, we have measured the $I-V$ curves as a function of gate voltage (V_g) between electrodes 2 and 3 at 288, 77, and 4.2 K, as shown in Figs. 3(a), 3(b), and 3(c), respectively. The insets show the corresponding source–drain current change as a function of V_g in the range of ± 10 V. The gate modulation curves of the other electrodes, for example, 3-4, 4-5, and 1-2 show also similar behaviors as that of the electrodes 2-3. The $I-V$ curve at room temperature exhibits linear behavior with resistance of 3 MΩ at zero gate voltage. Application of positive gate voltage progressively increases the conductance, which is a signature of an n-type field-effect transistor. Such an n-doped electrical property is known to result from nitrogen vacancies.[17] As the temperature is lowered to 77 K, the $I-V$ characteristics become slightly nonlinear and a pronounced n-type gating effect is exhibited, as shown in Fig. 3(b). As the temperature is lowered further to 4.2 K, the $I-V$ curve becomes highly nonlinear and the n-type gating effect becomes much more pronounced, as shown in Fig. 3(c). At a temperature of 4.2 K with zero gate voltage, the $I-V$ curve exhibited an insulating region of $|V|<150$ mV. Positive gate voltage suppresses the insulating region, giving $|V|<70$ mV at $V_g=+10$ V, while negative gate voltage expands the insulating region, giving $|V|<500$ mV at $V_g=-10$ V.

The n-type gate response of the GaN nanowire can be understood by the band diagram, as shown in the lower inset of Fig. 3(c). If an n-type semiconductor is in contact with a metal electrode, the energy band of the n-type semiconductor is bent to align its Fermi level to that of the metal.[18] When a positive gate voltage is applied, the conduction band of the n-type semiconductor is pulled downward, giving an increased density of states near the Fermi level and, as a result, an enhanced conductance. A negative gate bias voltage, on the other hand, raises the bands upward and suppresses the conductance of the nanowire.

As was mentioned previously, the temperature dependence of the linear resistance is fitted well to the thermal activation form at the high-temperature region, but noticeable deviation was observed at the low-temperature region. Activation energy E_a, obtained from the fitting of the high-temperature conductance to the Arrhenius form, would be related to the energy difference (E_{CF}) between conduction-band edge of the nanowire (E_C) and the Fermi level of the metal electrode, $E_{CF}=E_C-E_F$. E_{CF} acts as an energy barrier to overcome an electron to pass through the nanowire. At high temperatures, thermal energy k_BT becomes comparable to or larger than energy barrier E_{CF}, and the thermionic emission would be a dominant transport mechanism. At low temperatures, on the other hand, the thermionic emission current is suppressed and another transport mechanism, like the quantum tunneling of electrons through the energy barrier,

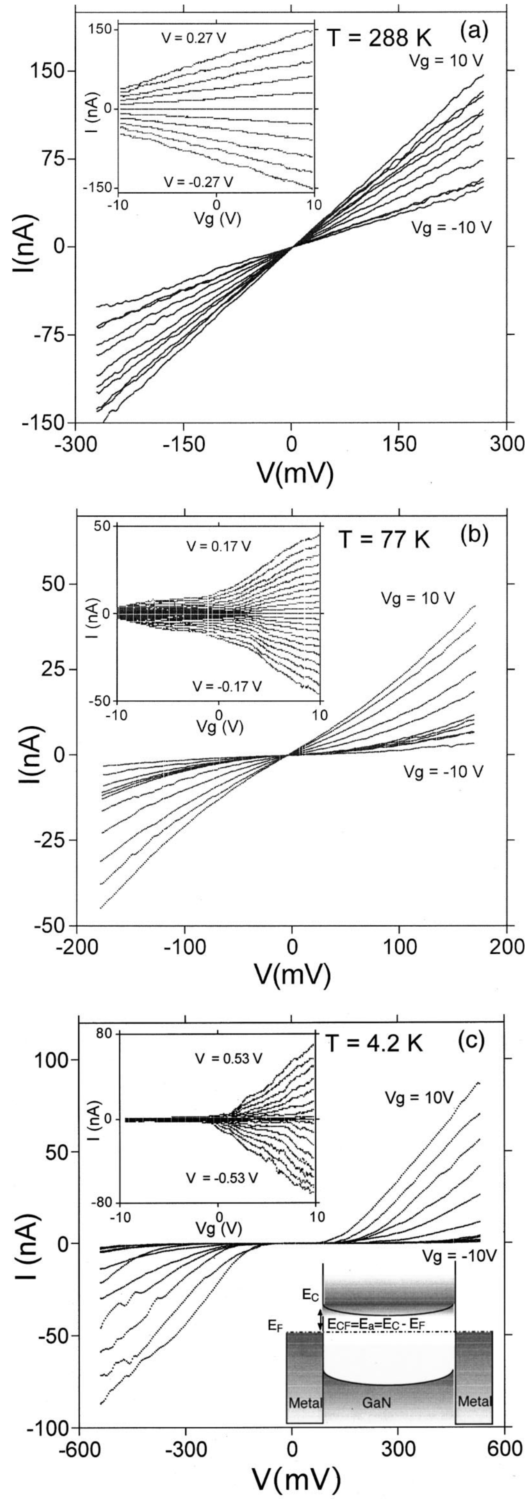

FIG. 3. $I-V$ curves as a function of V_g between electrodes 2 and 3 at (a) 288 K, (b) 77 K, and (c) 4.2 K, respectively. The gate bias varies from $+10$ to -10 V. Insets show the corresponding source–drain current changes as a function of V_g. The lower inset in (c) represents the schematic band diagram for the n-type GaN wire and metal electrodes.

may not be neglected. In general, the tunneling effect becomes important at low temperatures and low bias voltages for a highly doped semiconductor. The deviation of zero-bias conductance to the thermal activation form, as shown in the lower inset of Fig. 2, is a manifestation of the importance of a transport mechanism other than thermionic emission at low temperatures. The non-negligible effect of tunneling through the contact barrier at low temperatures was also reported in the semiconducting single-walled CNT system with metal contacts.[19]

The carrier mobility of the nanowire can be estimated from the gate modulation characteristics with the relation, $dI/dV_g = \mu(C/L^2)V$, where μ is the carrier mobility and L is the nanowire length (330 nm). The capacitance is given by $C \approx 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$, where h is the thickness of the SiO_2 layer (500 nm) and r is the nanowire radius (15 nm). The room-temperature carrier mobility is estimated to be about $2.15\ cm^2/V\,s$ at a bias voltage of $V = 0.27$ V. Although this value is comparable to that of a B-doped silicon nanowire,[5] it is ten times smaller than that of the single-walled CNT reported by Martel *et al.*[1] and is considerably smaller than the electron mobility ($\mu = 380\ cm^2/V\,s$) of bulk GaN crystal.[18] Such a small mobility suggests the highly diffusive nature of electron transport possibly due to defects, disorder, and interface scattering. It is also believed that the enhanced scattering due to a smaller diameter also contributes in part to the reduced mobility.

In summary, we have synthesized high-quality crystalline GaN naowires and studied the electrical transport properties for individual nanowires. GaN nanowires show a pronounced n-type field effect due to nitrogen vacancies. At high temperatures, the conductance change by a gate voltage mostly originates from the nanowire itself. The tunneling effect through the contact energy barrier between the nanowire and metal electrodes becomes important as the temperature is lowered. The estimated electron mobility in the GaN nanowire is about $2.15\ cm^2/V\,s$ at $V = 0.27$ V, which is about 200 times smaller than that of GaN bulk crystal.

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